In the Specification

The following is a marked-up version of the specification with the language that is underlined ("___") being added and the language that contains strikethrough ("—" or "[[ ]]") being deleted:

For the paragraph beginning at page 1, paragraph [0004]:

Two basic approaches to VGA design, or generally, design of systems using VGAs, include signal summing-VGAs (e.g., a particular topology for a VGA that sums two different current paths with two different gains) and soft-switching degeneration (e.g., the degeneration being degeneration elements comprising a parallel configured, variable resistance at the emitter terminals of an amplifier, and the soft-switching including controlling the variable resistance using control voltage circuitry that operates over a continuum range of voltage values (analog) as opposed to discrete (digital) control voltage values[[)]], both of which are discussed in the following IEEE publications that are herein incorporated by reference: "A low power low noise accurate linear-in-dB variable gain amplifier with 500 MHz bandwidth," S. Otaka, et al., IEEE J. Solid State Circuits, pp. 1942-1947, Dec. 2000, and "Adaptive analog IF signal processor for a wide band CMOS wireless receiver," F. Behbahani et al., IEEE J. Solid State Circuits, pp. 1205-1217, Aug. 2001.

For the paragraph beginning at page 4, paragraph [0008]:

The closed loop gain is given by:

$$V_{out} = (V_{ref} - V_{fb}) A_{err} A_{BBVGA} A_{PA} A_{mix} \qquad (1)$$

where Aerr, ABBVGA, Amix, and APA are the gains of the error amplifier 102, BB VGA 104, IF mixer 108, and the PA 106, respectively. In other words, (Vref - Vfb) is amplified in the feedforward path. Further, Vfb is the output voltage (Vout) multiplied by the gain in the feedback path (which includes the gain of the IF mixer 108, represented by Amix, and the gain of the IF VGA 110, represented by AIFVGA). Thus,

$$V_{fb} = V_{out} A_{IFVGA} A_{mix} \tag{2}$$

$$\frac{V_{out}}{V_{ref}} = \frac{A_{BBVGA} A_{PA} A_{err}}{1 + A_{BBVGA} A_{mix} A_{PA} A_{err} A_{IFVGA}} \tag{3}$$

Assuming the "1" is negligible in the denominator, the open loop gain, T, is approximated as:

$$T = A_{BBVGA} A_{PA} A_{mix} A_{err} A_{IFVGA} \tag{4}$$

Since the gain of the IF VGA 110 and the BB VGA 104 are inversely proportional to one another, the open loop gain is constant versus VGA gain.

If T>>1, the then the closed loop gain is reduced to:

$$\frac{V_{out}}{V_{ref}} \cong \frac{1}{A_{IFVGA}} \tag{5}$$

Therefore, if the gain in the feedforward path is large, the output (Vout) is controlled by the gain in the feedback path. The output of the PA 106 is directly related to the gain (and

amplitude variation) of the IF VGA 110. For example, if the IF VGA gain is large, the PA output power is small. If the IF VGA gain is small, the PA output power will be large.

For the paragraph beginning at page 4, paragraph [0010]:

FIGS. 1B and 1C are combination schematic and block ~~schematic~~ diagrams of an IF VGA 110a and a BB VGA 104a that operates in conjunction with the IF VGA 110a. The "a" signifies one embodiment for the respective IF VGA 110 and the BB VGA 104 shown in FIG. 1A. The IF VGA 110a of FIG. 1B includes differential pair transistors 124 and 126 that receive a differential input over connection 120 (FIG. 1A) at base terminals 125 and 127, respectively. At the emitter terminal of the differential pair transistors 124 and 126 is an emitter degeneration element 128 that comprises one or more n-channel MOSFETs (or NMOS transistors) functioning as a variable resistance. Degeneration elements include a resistance at the emitter or source terminals of transistors comprising the input stage of an amplifier. The resistance can include resistance from transistors and/or resistors (collectively resistive elements). Degeneration elements often ~~improves~~ improve linearity with some reduction in gain and noise. The equivalent resistance of the NMOS transistors of the emitter degeneration element 128 are changed (varied) (via soft-switching, which uses a continuous range (0 – 100%) of voltage values from the control voltage circuitry to create a smooth change in gain, or discrete (0 or 100%, or digital) switching to create a "stair-case" change in gain) via application of control voltage VC1 to control terminal 132. VC1 is coupled to a resistive network (not shown), and increased or decreased to provide staggered voltages to enable the equivalent resistance of one or more NMOS transistors to be changed. As the number of NMOS transistors is increased, the resulting equivalent resistance of the emitter degeneration element 128 is decreased, providing for a variation in gain.

For the paragraph beginning at page 5, paragraph [0011]:

The IF VGA 110a also includes a collector load 130 at the collector ~~terminal~~ terminals of the differential pair transistors 124 and 126. The collector load 130 comprises one or more p-channel MOSFETs (or PMOS transistors) functioning as a variable resistance. The output of the collector load 130 is provided over connection 122 (FIG. 1A). The equivalent resistance of the PMOS transistors of the collector load 130 is also varied through the application of a control voltage VC2 to control terminal 134. Power is supplied via a direct current (DC) power source (not shown) providing a voltage VCC to power terminal 136, which provides a supply voltage to the differential pair transistors 124 and 126, among other components as described below.

For the paragraph beginning at page 5, paragraph [0014]:

FIGS. 2A and 2B are combination schematic and block ~~schematic~~ diagrams that illustrate another approach to configuring a VGA system comprising an IF VGA 110b and a BB VGA 104b. The "b" signifies another embodiment for the respective IF VGA 110 and the BB VGA 104 shown in FIG. 1A. The IF VGA 110b comprises differential pair transistors 224 and 226 that receive a differential input over connection 120 at base terminals 225 and 227, respectively. Resistors 254 and 256 are coupled between the power terminal 136 that receives a supply voltage VCC and collector terminals of each of the differential pair transistors 224 and 226. The resistors 254 and 256 comprise a collector load. The IF VGA 110b also includes an emitter degeneration element 228 comprising one or more NMOS transistors. The emitter degeneration element 228 is controlled by the application of a control voltage VC1 to control terminal 132.

For the paragraph beginning at page 6, paragraph [0016]:

FIG. 3 is a schematic view of the IF VGA 110a. A similar structure can be used for the BB VGA 104a (FIG. 1C). In a typical portable transceiver system, one or more stages of an IF VGA and/or a BB VGA are implemented (e.g., cascaded, providing the same or different gains) to provide a broader gain range. An input signal is applied to differential input terminals 302 and 314 over connection 120 (FIG. 1A). Input terminal 302 is connected to the base terminal 125 of differential pair transistor 124 via connection 304. Input terminal 314 is connected to base terminal 127 of a differential pair transistor 126 via connection 316. In addition to the base terminal 125, the differential pair transistor 124 includes a collector terminal 308 and an emitter terminal 312. Similarly, the differential pair transistor 126 includes a collector terminal 320 and an emitter terminal 324, in addition to the base terminal 127.

For the paragraph beginning at page 10, paragraph [0025]:

The curves labeled 404 show increasing gain with an increase in differential input control voltage, and correspond to changes in power source supply voltage (again, further exacerbated if the BB VGAs are subject to variations in manufacturing process and/or ambient temperature). The BB VGA curves 404 have a range of approximately 30 dB down to –30 to –35 dB over the range in differential input control voltage. One goal in the design of VGA systems is to keep the combined gain variation of the IF VGA and BB VGA within a limited range. FIG. 4B shows the simulated, combined gain variation curves 406 for the IF VGA and BB VGA used to develop the curves 402 and 404 shown in FIG. 4A. The combined gain variation curves 406 range anywhere from 31 dB down to 16 dB. Even within the desired linear operating range shown between points A and B, the variation in output

power as a result ~~in~~ of changes in supply voltage (e.g., VCC) for a given differential input control voltage is significant.

For the paragraph beginning at page 11, paragraph [0032]:

FIGS. 2A and 2B are combination schematic and block ~~schematic~~ diagrams that illustrate another exemplar configuration for an IF VGA and a BB VGA.